IBM field engineering announcement

SYSTEM/360 MODEL 85

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The IBM System/360 Model 85 operates in the speed range between the System/360 Models 75 and 91. The functional organization of the Model 85 is equivalent to other models of the System/360; it shares the same instruction set and is upward-compatible with other members of the System/360 family.

The high performance of the Model 85 is attributed to:

- An 80-nanosecond processor cycle (0.08 usec).
- A 16-byte main storage word – 128 data bits.
- An 80-nanosecond, 16k byte buffer that provides an effective storage speed of 1/3 to 1/4 of the actual 1-microsecond main storage.
- A Read-Only Storage (ROS) for E-Unit control.
- A versatile Storage Control Unit (SCU) that can initiate storage references every processor cycle.
- Multiple instruction and operand buffers.
- Overlapped instruction and execution cycles.
- Parallel operation of fixed point or floating point instructions.
- New instructions that allow extended precision floating point operations for add, subtract, and multiply, as well as the rounding of floating point numbers to short and long operands.

Main Storage

Up to 4,096 bytes of main storage are available for the Model 85; the 2365 Processor Storage Model 5, for 512k and 1,024k bytes, and the 2385 Processor Storage Models 1 and 2, for 2,048k and 4,096k bytes. Both the 2365 Model 5 and the 2385 Models 1 and 2 produce a 16-byte quadruple word each 1.04-microsecond cycle. All Model 85 processor storage units have an error correction capability that corrects any single bit error with no lost processing time.

High-Speed Buffer

A 16k-byte (expandable to 24 or 32k), main storage buffer operates between main storage and the rest of the processor. Because this buffer cycles at an 80-nanosecond rate, the system works effectively with very high-speed storage; processing can therefore approach one instruction per processor cycle.

Channels

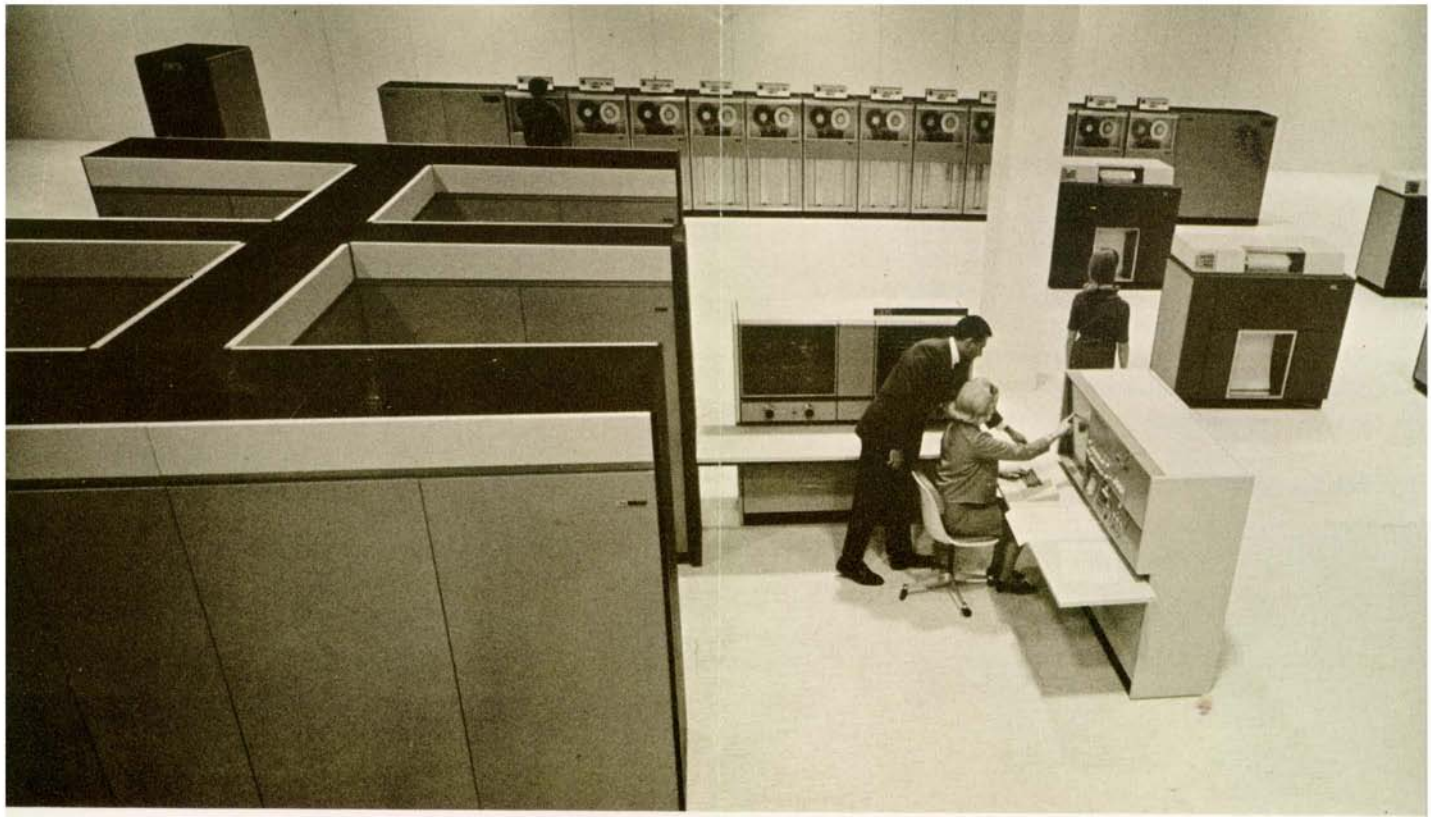
Existing 2860 Selector Channels and 2870 Multiplexer Channels are used with the Model 85.

Significant Maintenance Features

In addition to the functional packaging, logout, diagnose, failure detection, and parity checking features, Model 85 maintainability is enhanced by:

- *A CRT* to display every major register.
- *A Modified Microfiche Viewer* to display every significant control and status trigger.
- *A Hex-Entry Keyboard* to simplify manual data entry.
- *Microdiagnostics* to exercise the CPU at the microinstruction level and locate faults.
- *An Instruction Retry Facility* to allow a failing instruction to be automatically repeated.

PRINTED IN U.S.A. 223-2928-0



I-Unit

The I-Unit for the Model 85 prepares the instructions for the E-Unit. Up to three instructions can be queued and two storage operands can be buffered. Functional components for the I-Unit that contribute to the performance of the Model 85 include:

- Two 128-bit instruction buffers.
- Four 24-bit instruction address registers.
- A 24-bit, three-input addressing adder.

For branch instructions, as many as 16 bytes of instructions are fetched from both instruction streams.

E-Unit

The E-Unit executes instructions prepared by the I-Unit and is controlled by a Read-Only Storage (ROS). Functional components for the E-Unit that contribute to the performance of the Model 85 include:

- A parallel adder, 64 bits wide, that includes a 32-bit logical unit (AND, OR, OE).
- A parallel shifter that allows shifts of 0 to 63 positions, left or right, in a single processor cycle.
- A high-speed multiply unit (feature) that processes 12 bits per cycle in both fixed and floating point multiply operations.
- A serial adder that handles eight bits, binary or decimal, for executing SS operations and overlapped floating point exponent calculations.
- A local storage with simultaneous read-out paths.

ROS and WCS

The Read-Only Storage (ROS) and the Writable Control Storage (WCS) control E-Unit operations. The ROS is capacitive and contains 2,048 108-bit words. The WCS contains 515 108-bit words (expandable to 1,024 126-bit words). The WCS provides control storage for diagnostic purposes and for emulator capability. Both the ROS and the WCS have 80-nanosecond cycles.

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